REMARKS

Claims 1-8 and 12-23 remain pending in the application, claims 10 and 11 being canceled herein.

35 USC 112 First Paragraph Rejection of Claims 1-8, 10-16, 20, 21 and 23

In the Office Action, claims 1-8, 10-16, 20, 21 and 23 were rejected as allegedly containing subject matter which is not described in the specification under 35 USC 112. In particular, the language in claims 1, 7, 13, 20 and 23, i.e., a second agent lacking a dedicated clock, is alleged to lack support in the specification. Claims 10 and 11 are canceled herein, making the rejection moot in this regard. Otherwise, the Applicants respectfully traverse the rejection.

To further the prosecution of the present application, Applicants have amended the claims to not utilize the language "a second agent lacking a dedicated clock" cited by the Examiner. Thus, it is believed that the Examiner will agree that all claims are in full conformance with 35 USC 112. Accordingly, the Applicants respectfully request that the rejection of claims 1-8, 10-16, 20, 21 and 23 under 35 USC 112 be withdrawn.

Claims 17-19 and 22 over Persaud

Claims 17-19 and 22 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated be Persaud et al., UK Patent Application No. GB2074762 ("Persaud"). The Applicants respectfully traverse the rejection.

Claims 17-19 and 22 recite accessing external non-dedicated shared **synchronous** memory from a second agent based on a representation of a memory access clock signal that is in synchronism and in-phase with a memory access clock signal.

Persaud discloses an out-dated and rudimentary technique for synchronizing agents each accessing their own dedicated asynchronous dynamic random access memory (DRAM). A master one of the agents is given special access to interrupt operations by a slave agent and interject a memory access to the DRAM dedicated to that slave.

According to Persaud, the master generates synchronizing signals applied over a backplane to each of the slave agents. (Persaud, page 1, lines 45-46). According to Persaud, because all the processors are synchronized to the master processor, when the master does access a slave's dedicated memory, it has to inhibit operation of the respective slave processor. (Persaud, page 1, lines 46-48)

The memory which is being accessed in Persaud is asynchronous, DRAM (see, e.g., DRAM element 190, Fig. 5). This asynchronous DRAM requires a read/write signal that is generated either locally (LOCAL R/W) or by the master (BUS R/W).

Disadvantages of asynchronous DRAM are discussed at length in the background section of the current application. In particular, as explained in the text of the present application, increasing demands of high-end processors have obsoleted asynchronous DRAM. (See, e.g., specification, page 2, lines 7-10)

Synchronous memory circuit designs are based on state machine operation instead of level/pulse width driven as in conventional asynchronous memory devices (Id at lines 10-12)

The bottom line is that Persaud is very old late 1970s technology based on the use of level/pulse driven (e.g., R/W) signals. There is little similarity to today's synchronous memory systems. Moreover, one of ordinary skill in the art designing a computer system today would not have looked to art generated in the late 1970s for improvements.

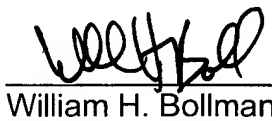
Simply put, Persaud fails to disclose synchronous memory, much less the use of synchronized clock signals between a plurality of agents accessing the same synchronous memory, as claimed by claims 17-19 and 22.

Accordingly, for at least all the above reasons, claims 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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